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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/519,069	03/03/2000	Gary A. Frazier	RAYT:009 (Case no. 37323)	7415

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EXAMINER	
NGUYEN, HUY D	

ART UNIT	PAPER NUMBER
2681	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/519,069	FRAZIER, GARY A.	
	Examiner	Art Unit	
	Huy D. Nguyen	2681	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/20/2004 have been fully considered but they are not persuasive.

In response to the arguments by applicants in the remarks, the examiner states that ~~since~~ claims do not specify how the clock circuitry is coupled to the delay circuit. The clock circuitry could be directly connected to the ADC via one pin and connected to the delay circuit via another pin; it could be connected to the ADC via the delay circuit. Therefore the teaching of Lam reads on the claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-38, 42-63 are rejected under 35 U.S.C. 102(e) as being anticipated by Lam (U.S. Patent Application Publication No. 2002/0013133 A1).

Regarding claims 1, 9, 17, 25, 33, 35, 42, 48, 53, 59, Lam teaches a digital phased array transceiver for receiving and transmitting electromagnetic energy, comprising: a plurality of antenna elements capable of receiving and transmitting electromagnetic energy; a receive module coupled to each of the plurality of antenna elements, each receive module including an

analog to digital converter controlled by a clock signal generated by clock circuitry coupled to a programmable delay circuit, wherein each programmable delay circuit delays a base clock signal from the clock circuitry by a desired amount so that a receive direction of the plurality of antenna elements may be electronically controlled; and a transmit module coupled to each of the plurality of antenna elements, each transmit module including a digital to analog converter controlled by a clock signal generated by clock circuitry coupled to a programmable delay circuit, wherein each programmable delay circuit delays a base clock signal from the clock circuitry by a desired amount so that a transmit direction of the plurality of antenna elements may be electronically controlled (paragraphs 0004, 0009, 0011, 0013, 0045, 0066).

Regarding claims 2, 10, 18, 26, 43, 49, 54, 60, Lam teaches the digital phased array receiver of claim 1, wherein each analog to digital converter has a multiple bit digital value as an output (paragraph 0070).

Regarding claims 3, 11, 19, 27, 44, 50, 55, 61, Lam teaches the digital phased array receiver of claim 1, wherein each analog to digital converter is a single bit digital value as an output (paragraph 0070).

Regarding claims 4, 20, Lam teaches the digital phased array receiver of claim 1, further comprising multiple data conversion circuits coupled to receive the output of each analog to digital converter at a first clock rate and having an output signal at a second clock rate (paragraphs 0070, 0080).

Regarding claims 5, 21, Lam teaches the digital phased array receiver of claim 4, wherein the first clock rate matches the base clock signal and the second clock rate is slower than the first clock rate (paragraphs 0070, 0080).

Regarding claims 6, 12, 22, 28, 45, 51, 56, 62, Lam teaches the digital phased array receiver of claim 1, wherein an amount of delay provided by each delay circuit is programmable (paragraph 0013).

Regarding claims 7, 23, 46, 57, Lam teaches the digital phased array receiver of claim 6, wherein the plurality of antenna elements are grouped into sets of antenna elements and wherein each antenna element within the same set has the same amount of programmed delay (paragraphs 0013, 0049).

Regarding claims 8, 16, 24, 32, 34, 36, 47, 52, 58, 63, Lam teaches the digital phased array receiver of claim 1, wherein the electromagnetic energy is radio frequency energy (paragraphs 0005, 0049).

Regarding claims 13, 29, Lam teaches the digital phased array receive-path module of claim 12, wherein the delay circuit is controlled by a digital word provided by a control register that may be loaded with a desired delay value (paragraph 0044).

Regarding claims 14-15, 30-31, Lam teaches the digital phased array receive-path module of claim 9, further comprising synchronization circuitry coupled to the analog to digital converter to receive and then output data from the analog to digital converter at an output clock rate (paragraphs 0056, 0066, 0083).

Regarding claim 37, Lam teaches the digital phased array of claim 35, wherein the programmable delay circuitry comprises a first time delay circuit having a clock output for the analog to digital converter and a second time delay circuit having a clock output for the digital to analog converter (paragraphs 0044, 0049, 0070).

Regarding claim 38, Lam teaches the digital phased array of claim 35, wherein the programmable delay circuitry comprises a single time delay circuit having a single clock output for both the analog to digital converter and the digital to analog converter (paragraphs 0044, 0070).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lam in view of Linstrom et al (U.S. Patent No. 6,351,247).

Regarding claim 39, Lam teaches the digital phased array of claim 35 except that the programmable delay circuitry comprises digitally programmable micro-electromechanical switch (MEMS) phase shifters. However, the preceding limitation is taught in Linstrom et al. (Col. 2, lines 1-13). It would have been obvious to one of ordinary skill in the art, at the time of invention, to use digitally programmable micro-electromechanical switch (MEMS) phase shifters as taught by Linstrom et al. to meet specific design criteria.

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lam in view of Schuss et al (U.S. Patent No. 4,743,914).

Regarding claim 40, Lam teaches the digital phased array of claim 35 except that the programmable delay circuitry comprises digitally programmable diode phase shifters. However, the preceding limitation is taught in Schuss et al. (Col. 3, lines 66-68; Col. 5, lines 1-8). It would have been obvious to one of ordinary skill in the art, at the time of invention, to use diode phase shifters as taught by Schuss et al. to meet specific design criteria.

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lam in view of Komarek et al (U.S. Patent No. 5,907,517).

Regarding claim 41, Lam teaches the digital phased array of claim 35 except that the programmable delay circuitry comprises digitally programmable field effect transistor (FET) switching devices. However, the preceding limitation is taught in Komarek et al. (table III). It would have been obvious to one of ordinary skill in the art, at the time of invention, to use programmable field effect transistor (FET) switching devices as taught by Komarek et al. to meet specific design criteria.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Huy D. Nguyen whose telephone number is 571-272-7845. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on 703-306-0003. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HN

Huy Nguyen

EMMANUEL L. MOISE
SUPERVISORY PATENT EXAMINER